Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VIN**
2. **TEMP OUT**
3. **GROUND\***
4. **GROUND\***
5. **TRIM**
6. **VOUT FORCE†**
7. **VOUT SENSE†**

**.085”**

**7**

**6**

**4 5**

**1**

**2**

**3**

**.062”**

**DIE ID**

**1802Y**

**NOTES:**

**\*Pads 3 and 4 must both be bonded to GROUND.**

**†VOUT FORCE and VOUT SENSE are bonded together at the LOAD.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 1802Y**

**APPROVED BY: DK DIE SIZE .062” X .085” DATE: 8/25/21**

**MFG: ANALOG DEVICES THICKNESS .021” P/N: REF43NBC**

**DG 10.1.2**

#### Rev B, 7/19/02